AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application.

1. (currently amended) An apparatus for processing information wherein processing operations include a plurality of tasks, at least one of the plurality of tasks having a critical section, the apparatus comprising:

a first processing element, said first processing element including:

a critical section end detector, and

a critical section end signal generator coupled to said critical section end detector; and

a second processing element, said second processing element coupled to said first processing element and including:

a critical section detector, and

a critical section processing controller, said critical section processing controller responsive to a critical section end signal received from said first processing element.

2. (original) The apparatus of claim 1, said second processing element further including a counter, said critical section processing controller incrementing said counter in response to a critical section end signal.

3. (original) The apparatus of claim 1, said second processing element further including a counter, said critical section processing controller decrementing said counter based on the detection of a critical section.

4. (original) The apparatus of claim 1, said second processing element further including a counter, said critical section processing controller suspending issuing instructions wfen said counter includes a value less than a threshold.

5. (original) The apparatus of claim 1, wherein said first processing element sends a critical section end signal to said second processing element in response to processing an instruction identifying an end of a critical section.

6. (original) The apparatus of claim 1, wherein said second processing element suspends processing a task in response to said critical section detector detecting a critical section.

7. (original) The apparatus of claim 1, wherein said critical section processing controller suspends issuing instructions to an instruction unit in response to said critical section detector detecting a critical section.

8. (original) The apparatus of claim 7, wherein a critical section instruction identifies a beginning of a critical section in the task at said second processing element.

9. (original) The apparatus of claim 7, wherein the critical section includes an instruction that accesses a shared variable.

10. (original) The apparatus of claim 7, wherein the critical section includes an instruction that accesses a shared peripheral.

11. (original) The apparatus of claim 1, wherein said critical section end signal generator generates a critical section end signal in response to said critical section end detector.

12. (original) An apparatus for processing multiple data elements wherein processing operations include a plurality of tasks, one or more of which having a critical section, the apparatus comprising:

a ring of processing elements;

a first processing element in said ring of processing elements, said first processing element including:

a critical section end detector, and

a critical section end signal generator; and

a second processing element in said ring of processing elements, said second processing element coupled to said first processing element, and including:

a critical section detector, and

a critical section processing controller, said critical section processing controller responsive to a critical section end signal received from said first processing element.

13. (original) The apparatus of claim 12, wherein said first processing element sends a critical section end signal in response to processing an instruction identifying an end of a critical section.

14. (original) The apparatus of claim 12, wherein said second processing element suspends processing a task in response to said critical section detector.

15. (original) The apparatus of claim 12, wherein said second processing element suspends processing a task at a critical section instruction.

16. (original) The apparatus of claim 12, wherein said first processing element and said second processing element are adjacent in said ring of processing elements.

17. (original) The apparatus of claim 16, wherein said first processing element is upstream from said second processing element in said ring of processing elements.

18. (original) The apparatus of claim 12, said second processing element further including a counter, said critical section processing controller incrementing said counter in response to a critical section end signal.

19. (original) The apparatus of claim 12, said second processing element further including a counter, said critical section processing controller decrementing said counter based on the detection of a critical section.

20. (original) The apparatus of claim 12, said second processing element further including a counter, said critical section processing controller suspending issuing instructions when said counter includes a value less than a threshold.

21. (currently amended) A method for processing tasks on multiple processing elements, comprising:

processing a first task on a first processing element;

inhibiting processing of a second task on a second processing element based on processing a critical section instruction at the second processing element;

receiving a critical section end signal at the second processing element from the first processing element, the critical section end signal indicating completion of processing of a critical section of a task at ~~another~~ the first processing element; and

resuming processing the second task at the second processing element based on the critical section end signal.

22. (original) The method of claim 21, wherein said inhibiting occurs substantially at a beginning of a critical section of the task at the second processing element.

23. (original) The method of claim 21, wherein said resuming occurs substantially at an end of a critical section of the task at the first processing element.

24. (original) The method of claim 21, wherein the first processing element and the second processing element are associated with a single network connection during the processing of the task associated with the first processing element and the task associated with the second processing element, respectively.

25. (original) The method of claim 21, wherein the first processing element and the second processing element are associated with different network connections during the processing of the task associated with the first processing element and the task associated with the second processing element, respectively.

26. (currently amended) The method of claim 21, wherein said receiving ~~sending~~ occurs in response to processing an critical section end instruction.

27. (currently amended) The method of claim 21, wherein said receiving ~~sending~~ occurs in response to detecting a critical section end instruction.

28. (currently amended) The method of claim 2 1, further comprising storing data to a memory shared by the first processing element and the second processing element, said receiving ~~sending~~ the critical section end signal occurring in response to said storing.

29. (original) The method of claim 21, wherein the task at the first processing element and the task at the second processing element are associated with a single network connection.

30. (original) The method of claim 21, wherein the task at the first processing element and the task at the second processing element are associated with different network connections.

31. (original) The method of claim 21, wherein the task at the first processing element and the task at the second processing element are associated with ordered data elements.

32. (currently amended) The method of claim 21, wherein said receiving ~~sending~~ occurs in response to processing an instruction identifying an end of a critical section.

33. (original) The method of claim 21, wherein said inhibiting occurs in response to processing an critical section instruction.

34. (original) The method of claim 33, wherein the critical section instruction identifies a beginning of a critical section in the task at the second processing element.

35. (original) The method of claim 33, wherein the critical section instruction is an instruction accessing a shared variable.

36. (original) The method of claim 33, wherein the critical section instruction is an instruction accessing a shared peripheral.

37. (currently amended) A method for controlling access to shared resources while processing network data elements on multiple processing elements, the method comprising:

detecting a critical section instruction among a series of instructions to be executed while processing a network data element at a first processing element;

prior to executing the critical section instruction, checking an end critical section signal counter associated with a second processing element; and

suspending execution of the critical section instruction when said end critical section signal counter is not above a threshold value.

38. (original) The method of claim 37, wherein said suspending occurs substantially at a beginning of a critical section of a task at the first processing element..

39. (original) The method of claim 38, wherein said resuming occurs substantially at an end of a critical section of a task at second processing element.

40. (original) The method of claim 37, further comprising resuming execution of the critical section instruction when the end critical section signal counter is determined to be above a threshold value.

41. (original) The method of claim 37, further comprising incrementing the end critical section signal counter upon receipt of an end critical section signal.

42. (original) The method of claim 37, wherein said suspending occurs in response to 2 processing a critical section instruction.

43. (original) The method of claim 42, wherein the critical section instruction identifies a beginning of a critical section in the task at the first processing element.

44. (original) The method of claim 43, wherein the critical section includes an instruction that accesses a shared variable.

45. (original) The method of claim 43, wherein the critical section instruction includes an 2 instruction that accesses a shared peripheral.

46. (original) A method for performing parallel processing, comprising:
suspending processing of a task at a first processing element in response to detecting a beginning of a critical section of the task; and
resuming processing of the task at the first processing element in response to a critical section end signal received from a second processing element.

47. (original) The method of claim 46, wherein the first processing element and the second processing element are coupled within a ring of processing element.

48. (original) The method of claim 46, further comprising prior to said suspending, checking an end critical section signal counter associated with a second processing element.

49. (original) The method of claim 48, wherein said suspending occurs in response to determining the end critical section signal counter is not above a threshold value.

50. (original) The method of claim 46, further comprising receiving an end critical section signal from a second processing element.

51. (original) The method of claim 46, further comprising incrementing an end critical section signal counter associated with the first processing element in response to receiving an end critical section signal from the second processing element.

52. (currently amended) The method of claim 46, wherein the first processing element and the second processing element are adjacent within a ring of processing elements.

53. (original) An apparatus for processing multiple data elements wherein processing operations include a plurality of tasks, one or more of which having a critical section, the apparatus comprising:

a ring of processing elements;

a first processing element in said ring of processing elements, said first processing element including:

a critical section operative state element, and

a critical section end signal generator; and

a second processing element in said ring of processing elements, said second processing element coupled to said first processing element, said second processing element including a critical section detector.

54. (original) The apparatus of claim 53, wherein said first processing element is adjacent to said second processing element in said ring of processing elements.

55. (original) The apparatus of claim 53, wherein said second processing element suspends processing a task at the beginning of a critical section.

56. (original) The apparatus of claim 55, wherein the critical section includes an instruction that accesses a shared variable.

57. (original) The apparatus of claim 55, wherein the critical section includes an instruction that accesses a shared peripheral.

58. (currently amended) A method for controlling access to shared resources while processing network data elements on multiple processing elements, the method comprising:

detecting a critical section instruction among a series of instructions to be executed while processing a network data element at a first processing element;

prior to executing the critical section instruction, checking a critical section processing controller associated with a second processing element; and

inhibiting execution of the critical section instruction when said critical section processing controller indicates that a critical section instruction should not be executed.

59. (currently amended) An apparatus for processing information wherein processing operations include a plurality of tasks, one or more of which having a critical section, the apparatus comprising:

a ring of processing elements;

a first processing element in said ring of processing elements, said first processing element including:

a critical section end detector, and

a critical section end signal generator; and

a second processing element in said ring of processing elements, said second processing element coupled to said first processing element, and including:

a critical section end signal counter, said critical section end signal counter responsive to a critical section end signal received from said first processing element,

a critical section detector, and

a critical section processing controller, said critical section processing controller responsive to said critical section end signal counter.